CLAIMS:

1. A chip stack comprising:

at least two carrier layers, each of the carrier layers including a first conductive pattern disposed thereon;

at least one thermal ring having a second conductive pattern disposed thereon and including at least two flow channels disposed therein, the thermal ring being disposed between the carrier layers, with the second conductive pattern being electrically connected to the first conductive pattern of each of the carrier layers; and

at least two integrated circuit chips electrically connected to respective ones of the first conductive patterns, one of the integrated circuit chips being circumvented by the thermal ring and disposed between the carrier layers;

the flow channels being operative to facilitate the circulation of air over the integrated circuit chip disposed between the carrier layers.

2. The chip stack of Claim 1 further comprising:

a transposer layer having a third conductive pattern disposed thereon;

the first conductive pattern of one of the carrier layers being electrically connected to the third conductive pattern.

3. The chip stack of Claim 2 wherein:

each of the carrier layers defines opposed top and bottom surfaces; and

the first conductive pattern of each of the carrier layers comprises:

a first set of carrier pads disposed on the top surface;

a second set of carrier pads disposed on the top surface and electrically connected to

respective ones of the carrier pads of the first set; and

a third set of carrier pads disposed on the bottom surface and electrically connected to respective ones of the carrier pads of the second set;

the integrated circuit chips being disposed upon respective ones of the top surfaces and electrically connected to at least some of the carrier pads of respective ones of the first sets, with the carrier pads of the second set of one of the carrier layers being electrically connected to the second conductive pattern, and the carrier pads of the third set of one of the carrier layers being electrically connected to the second conductive pattern.

4. The chip stack of Claim 3 wherein:

the thermal ring defines opposed top and bottom surfaces; and

the second conductive pattern comprises:

a first set of ring pads disposed on the top surface of the thermal ring; and

a second set of ring pads disposed on the bottom surface of the thermal ring and electrically connected to respective ones of the ring pads of the first set;

the thermal ring being disposed between the carrier layers such that the ring pads of the second set are electrically connected to respective ones of the carrier pads of the second set of one of the carrier layers, and the ring pads of the first set are electrically connected to respective ones of the carrier pads of the third set of one of the base layers.

5. The chip stack of Claim 4 wherein:

the transposer layer defines opposed top and

bottom surfaces; and

the third conductive pattern comprises:

a first set of transposer pads disposed on the top surface; and

a second set of transposer pads disposed on the bottom surface and electrically connected to respective ones of the transposer pads of the first set;

the carrier pads of the third set of one of the carrier layers being electrically connected to respective ones of the transposer pads of the first set.

6. The chip stack of Claim 5 wherein the transposer pads of the first set, the ring pads of the first and second sets, and the carrier pads of the second and third sets are arranged in identical patterns.

7. The chip stack of Claim 6 wherein:

the transposer and carrier layers each have a generally rectangular configuration defining opposed pairs of longitudinal and lateral peripheral edge segments;

the thermal ring has a generally rectangular configuration defining opposed pairs of longitudinal and lateral side sections;

the transposer pads of the first set extend along the longitudinal and lateral peripheral edge segments of the transposer layer;

the first and second sets of ring pads extend along the longitudinal and lateral side sections of the thermal ring; and

the second and third sets of carrier pads extend along the longitudinal and lateral peripheral edge segments of each of the carrier layers.

8. The chip stack of Claim 6 wherein:

each of the ring pads of the first set is

electrically connected to a respective one of the ring pads of the second set via a ring feed-through hole; and

each of the carrier pads of the second set is electrically connected to a respective one of the carrier pads of the third set via a carrier feed-through hole.

9. The chip stack of Claim 6 wherein the integrated circuit chips each comprise a package chip including:

a body having opposed, generally planar top and bottom surfaces; and

a plurality of conductive contacts disposed on the bottom surface of the body;

the conductive contacts of each of the packaged chips being electrically connected to respective ones of the carrier pads of the first set of a respective one of the first conductive patterns.

10. The chip stack of Claim 9 wherein the transposer pads of the second set, the carrier pads of the first set, and the conductive contacts are arranged in identical patterns.

11. The chip stack of Claim 9 wherein the body of each of the packaged chips and the thermal ring are sized relative to each other such that the top surface of the body circumvented by the thermal ring does not protrude beyond the top surface thereof.

12. The chip stack of Claim 9 wherein the packaged chips are each selected from the group consisting of:

a BGA device;

a fine pitch BGA device;

a CSP device; and

a flip chip device.

13. The chip stack of Claim 9 further comprising a heat sink attached to the top surface of the body of the packaged chip disposed between the carrier layers.

14. The chip stack of Claim 13 wherein the heat sink is attached to the body via an adhesive.

15. The chip stack of Claim 13 wherein the heat sink is fabricated from a layer of copper.

16. The chip stack of Claim 1 wherein:

the thermal ring defines a plurality of castellations; and

the flow channels are defined between each adjacent pair of the castellations.

17. The chip stack of Claim 16 wherein:

the thermal ring has a generally rectangular configuration defining opposed pairs of longitudinal and lateral side sections; and

the castellations are defined within each of the longitudinal side sections of the thermal ring.

18. The chip stack of Claim 16 wherein:

the thermal ring defines opposed, generally planar top and bottom surfaces, and is formed to have a ring thickness; and

the flow channels extend from the top surface of the thermal ring to a depth of approximately one-half the ring thickness.

19. The chip stack of Claim 16 wherein each of the flow channels has a generally rectangular cross-sectional configuration.

20. The chip stack of Claim 1 further comprising a heat sink attached to the integrated circuit chip disposed between the carrier layers.